Module and Application Description

PROCONTROL P

Binary and Analog Control Signal Processing

Control Module

for Binary Control Function 4-fold
for Analog Control Function 1- to 4-fold
for Applications with Redundant Design

83SR04 – E/R1310

Publication No.
D KWL 6323 94 E, Edition 05/95
Replacing D KWL 6323 94 E, Edition 06/94

Application

The module is used for stored–program binary and analog control tasks on the drive, group and unit control levels. It can be used for the following applications:

- Drive control of unidirectional drives
- Drive control of actuators
- Drive control of solenoid valves
- Binary function group control (sequential and logic)
- 3–step control
- Signal conditioning

The module is intended for use in connection with the process operator station.

The module can be operated in three different modes:

- Binary control mode
  (and analog basic functions)
  with variable cycle time
- Analog control mode
  (and binary control)
  with fixed, selectable cycle time
- Signal conditioning mode
  with fixed cycle time and disturbance bit output

The operating mode is selected by means of function block TXT1, which is the first to appear in the structure.

In the binary control mode, up to 4 binary function group controls or 4 drive controls, or combinations of drive and binary function group controls can be implemented for each module (noting the module cycle time).

In the analog control mode, a maximum of 4 analog control loops in the form of 3–step controllers – depending on the regulating time of the actuator – can be implemented for each module (see "Operating modes").

The module incorporates 4 hardware interfaces to the switchgear and the process.

This module is used to implement input and processing module redundancy in the PROCONTROL system.

Features

The module address is set automatically by plugging the module into the PROCONTROL station.

The telegrams received via the station–bus are checked by the module for error–free transfer via their parity bits.

The telegrams sent by the module to the bus are provided with parity bits to ensure error–free transfer.

The user program is filed in a non–volatile memory (EEPROM). It can be loaded and changed from the PDDS via the bus.

The module is ready for operation as soon as a valid user list is loaded.

For communication with the process and the switchgear, the module requires the following voltage:

USA/USB Operating voltage +24 V
branched internally into the following voltages:

- US11 Supply of contacts of process interface 1
- US21 Supply of contacts of process interface 2
- US31 Supply of contacts of process interface 3
- US41 Supply of contacts of process interface 4

The voltages US11 ... US41 are short–circuit–proof and designed to prevent any interaction.

The operating voltages and the external logic signals are related to reference conductor Z.

The following annunciations are indicated at the front of the module via light–emitting diodes:

- ST Disturbance
- SG Module disturbance

Light–emitting diode ST signals any disturbances in the module and in data communication with the module.
Light–emitting diode SG signals module disturbances only.

Processing is performed in parallel in the on−line and standby units. When a redundancy switchover is effected, this results in a bumpless transfer of the processing functions to the standby unit. This bumpless changeover is ensured by synchronizing the standby unit with the on−line unit by means of synchronizing telegrams.

Both on−line and standby units are self−monitoring. Any disturbances within the modules are signalled to the appropriate redundancy control module 88TR01 via the SSG line.

All process connections (connectors X21) of the individual modules belonging to a redundant pair are connected in parallel by appropriate wiring in the station.

The input resistors (burdens) are connected in the on−line unit and disconnected in the standby unit. This is also true for the process outputs and for the contact and transducer supplies from the module.

For diagnosis purposes, standby units transmit a sign−of−life telegram on the bus.

Module design

The module essentially consists of the following:

- Process interface
- Station−bus interface
- Processing section

Process interface

In the process interface, the process signals are adapted to the module−internal signal level.

Station−bus interface

In the station bus interface, the module signals are adapted to the bus. This essentially involves a parallel/serial conversion.

Processing section

In order to process the signals coming from the process and the bus, the module is provided with a microprocessor which works in conjunction with the following memory areas via a module−internal bus:

Contents		Type of memory
Operating program		EPROM
Function blocks		EPROM
User program	(Structure, address, parameter, limit value and simulation lists)	EEPROM
User program	(Structure, address, parameter, limit value and simulation lists)	RAM
History values		RAM
Current module input and output signals (shared memory)		RAM

The operating program enables the microprocessor to perform the basic operations of the module.

The memory for the function blocks contains ready programs for implementing the various functions.

The function blocks available in a particular operating mode are selected in such a way that the specified task can be performed without additional modules. For instance, in the analog control mode, it is possible to implement a superposed setpoint control in addition to the single−variable analog control.

All function blocks together with their inputs and outputs can be called by the user via the Programming, Diagnostic and Display System (PDDS).

The memory for the user program contains information as to:

- how the function modules are interconnected,
- which module inputs and outputs are allocated to the inputs and outputs of the function blocks,
- which constants are specified to the individual inputs of the function blocks,
- which parameters are specified to the individual inputs of the function blocks,
- which plant signals are allocated to the module inputs and outputs,
- which function blocks serve the process interfaces,
- which sets of limit values are allocated to the analog values,
- which calculated function results and module input and output signals are simulated.

This information is specified by the user according to the plant involved.

The complete user program is filed for normal operation in an EEPROM. For optimizing purposes, it possible to work with a modified copy of the user program in the RAM, which must then be taken over into the EEPROM upon completion of the optimizing process.

Settings (mainly in the analog control) can be either preset by the user directly at the appropriate function block inputs or alternatively specified in a separate parameter list.

When limit signals are formed by means of function block GRE, the limit values (4 per GRE) are specified in a limit value list.

Parameter and limit value lists can be changed (on line) at any time during operation. In this case, they are stored in the RAM or the assigned EEPROM, allocated to RAM and EEPROM operation respectively.

Data exchange between the module and the bus system proceeds via the memory for the module input and output signals. It serves to buffer the signals.

Structuring

During structuring, module inputs and outputs are allocated to the neutral inputs and outputs of the individual function blocks, or constants and parameters or outputs of other function blocks (calculated function results) are specified to the inputs of the function blocks. Structuring is performed on the basis of the data supplied by the user in the form of a socalled structure list.

The following limit values of the module have to be observed during structuring:

– max. no. of module inputs	287
– max. no. of simulatable module signals	32
– max. no. of module outputs	223
– max. no. of calculated function results	255
– max. no. of timers	136
– max. no. of parameters	80
– max. no. limit value sets	16
– max. no. of drive control functions (binary control, analog control) e.g. ASE, ASS, ASM and ASI functions	4
– max. no. of group control functions e.g. GSA and GSV functions	4
– max. no of lines in the structure list	2886
– Length of history values list (bytes)	2048
– Design of shared memory (see “ Addressing”)	

One line means one entry on the PDDS.

The proper procedure to be followed for structuring the function blocks is shown in the Function Block Descriptions.

Addressing

General

The signal exchange between the module and the bus system takes place via a shared memory. Here, incoming telegrams to be received by the module and calculated function results which are to leave the module are buffered.

The shared memory has send registers for telegrams to be transmitted and receive registers for telegrams to be received. Register numbers 0 to 63 are defined as send registers and numbers 64 to 199 as receive registers.

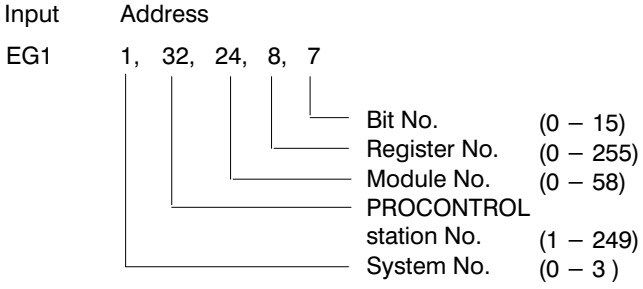
The allocation of the module input and output signals to the shared memory registers is determined from the PDDS on the basis of data supplied by the user.

The user data are in the form of address lists.

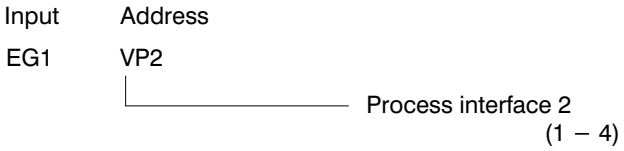
Address list for module inputs

In the address list for module inputs, the send location or the process interface associated with the signal to be received is allocated to each module input.

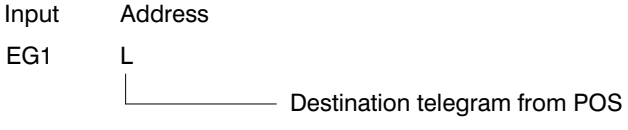
In the case of module inputs receiving their signal via the bus, addressing is done by allocating the send location address to EGn, e.g.



In the case of module inputs receiving their signal via the process interface, addressing is done by allocating the process interface to EGn, e.g.



In the case of module inputs receiving their signal from the process operator station, addressing is done by allocating L to EGn, e.g.:



The address list for inputs is translated by the PDDS into two module−internal lists, the "Bus address list" and the "Allocation list Module inputs".

The bus address list contains all telegrams to be used by the module, as well as the send location address and the receive register number.

Incoming telegrams whose addresses are included in the bus address list, are written to the receive register of the shared memory. Incoming telegrams whose addresses are not included in the bus address list are ignored by the module.

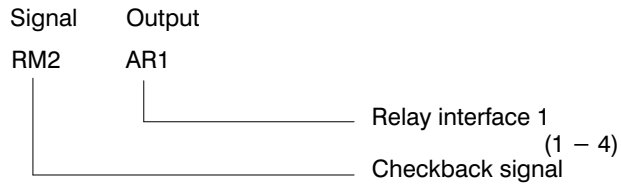
The allocation list for module inputs includes, for each module input, the associated receive register number and, in the case of binary values, also the bit position.

Address list for module outputs to the bus

In the address list for module outputs, a send register is defined for each signal to be output from the module, and a send bit is additionally defined in the case of binary signals, e.g.:

Addressing of the process interface for the relay outputs

In the case of module outputs supplying their signal to the relay interface, addressing is done in the structure list by allocation of ARn, with n denoting the number of the relay interface, e.g.:



Formation of address

The system and station addresses are set on the station bus coupling module (or on the station bus control module) and transmitted from this module to all other modules of a PROCONTROL station.

The module addresses are defined by connections on the backplane, so that each module is set automatically to the associated address while being plugged into a slot.

Sign−of−life telegram

On−line units transmit all telegrams as structured in the address list. Standby units transmit a sign−of−life telegram for diagnosis purposes. This is always register 0. If register 0 has been structured in the address list, the process telegram is transmitted with the appropriate data type. If register 0 has not been structured, a default telegram with data type 0 is transmitted. The sign−of−life telegram is transmitted cyclically.

Limit value list

The limit value list contains a set of 4 limit values for each of a maximum of 16 function blocks GRE (limit signal formation for one analog value). It is stored in the EEPROM and − in the case of RAM operation − in the RAM.

Limit value lists can be changed at any time from the PDDS and POS by way of a "Job memory" (RAM). Changes are stored in the EEPROM in the case of EEPROM operation, and in the RAM in the case of RAM operation. The limit value list is taken over from the RAM into the EEPROM, and vice versa, together with the user list.

Parameter list

The parameter list contains up to 80 values for parameters of the function blocks. It is handled and stored in the same way as the limit value list.

Simulation list

Using the PDDS, it is possible to ”simulate” up to 32 module signals (calculated function results, module inputs and outputs) by overwriting them with constant values. This simulation list is handled and stored in the same way as the limit value list.

Formation of events

The module is requested by the PROCONTROL system once every cycle to transmit the information filed in the send registers of the shared memory.

If any values change within the cycle time, this is treated as an event.

The module recognizes the following occurrences as events:

- Change of status in the case of binary values
- Change of an analog value by a permanently set threshold value of approx. 0.39 % and elapse of a time delay of 200 ms since the last transfer (cyclic or event).

If an event occurs, cyclic operation is interrupted and the new values are transferred to the bus with priority.

Disturbance bit evaluation, receive monitoring

The telegrams supplied via the bus may be provided with a fault flag on bit position 0. This fault flag is generated by the send module on the basis of plausibility checks, and the disturbance bit is set to ”1” in the event that specific disturbances are present (see Function Block Descriptions).

In order to be able to recognize errors during signal transfer, the module also incorporates a feature that monitors the input telegrams for cyclic renewal. If a telegram has not been renewed within a certain time, (e.g. due to failure of the send module), bit 0 is set to ”1” in the allocated receive register of the shared memory. In binary value telegrams, all the binary values are simultaneously set to “ 0”. In the case of analog values, the previous value is retained.

A set disturbance bit does not automatically involve a reaction in the receive module. If the disturbance bit of a telegram is to be evaluated, provision must be made for this during structuring.

In the ”Binary control” and ”Analog control” modes, disturbance bits of received telegrams can only be used within the module. They are not included in telegrams to be transmitted.

In the ”Signal conditioning” mode, disturbance bits are also included in transmitted telegrams.

Diagnosis and annunciation functions

Disturbance annunciations on the module

The following annunciations are signalled on the front of the module by light−emitting diodes (LED):

	Designation of LED
− Disturbance	ST
− Module disturbance	SG

Light−emitting diode ST signals all disturbances in the module and disturbances in data communication with the module.

Light−emitting diode SG signals module disturbances only.

Disturbance signals to the annunciation system

The annunciation system and the control diagnosis system CDS receive disturbance annunciation signals from the control module via the bus.

Diagnosis

All hardware and software functions of the module are monitored.

The incoming telegrams, the generation of the telegrams to be transmitted, and internal signal processing are monitored for errors in the processing section of the module (self−diagnosis).

In the event of a disturbance, the type of disturbance is filed in the diagnosis register and, at the same time, a general disturbance signal is sent to the PROCONTROL system.

If the annunciation ’process channel fault’ appears in the diagnosis register, this may be due to any of the following causes:

- Short−circuit at the contact supply outputs US11, US21, US31, or US41
- Short−circuit at the command outputs B11/B12/BV1, B21/B22/BV2, B31/B32/BV3, or B41/B42/BV4. (If any output commands are present for more than 5 sec, this will be interpreted as a disturbance of this category.)
- Open circuit at the command outputs B11/B12/BV1, B21/B22/BV2, B31/B32/BV3, or B41/B42/BV4. (If no output command is present, this will be interpreted as a disturbance of this category.)

If the annunciation ’processing fault’ appears in the diagnosis register, this may be due to any of the following causes:

- Invalid structuring
- Driver transistor for the command outputs B11/B12/BV1, B21/B22/BV2, B31/B32/BV3, or B41/B42/BV4 defective.

When requested, the module transfers a telegram with the data stored in the diagnosis register (register 246) (see Fig.1).

When the module’s SSG line is activated, this is interpreted as a module disturbance by the redundancy control module 88TR01 and indicated by the SG lamp on the module’s front panel.

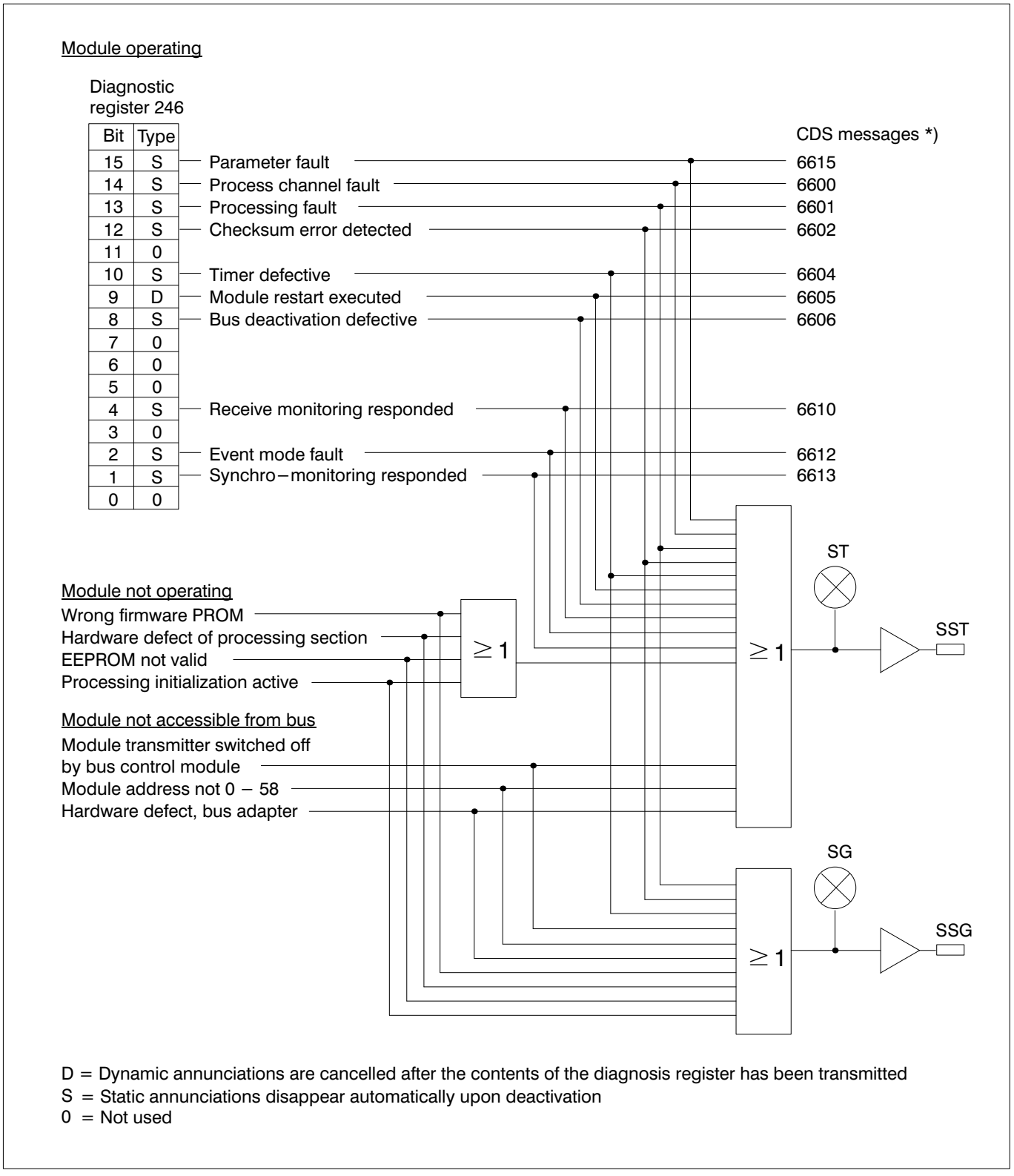


Figure 1: 83SR04 diagnosis messages

*) The control diagnosis system (CDS) provides a description for every annunciation number. This description provides, among other data:

- Information on cause and effect of the disturbance
- Recommendations for its elimination.

This makes for fast elimination of disturbances.

Operating statuses of the module

Initialization and bootstrapping with user lists

Initialization is accomplished either by plugging the module into its slot or after connection of the voltage.

The initialization process causes the module to assume a defined initial state. Light−emitting diodes ST and SG are on during this process.

No user program is available when the module is started up for the first time. As a result, the module signals “Processing fault”, and light−emitting diodes ST and SG are on.

As a first step, it is necessary to transfer the user program from the PDDS, via the bus, to the RAM of the module. If this operation is started with the structure list, the PDDS calls all other lists automatically. To avoid the transmission of incorrect lists, the PDDS checks the place of installation and the address before each transmission job. The module checks every incoming list for plausibility.

Now, the complete user program can be transferred to the EEPROM by a command from the PDDS.

Following this, the module is ready for operation, and the light−emitting diodes ST and SG are deenergized.

Normal operation

The module processes the user program filed in the EEPROM.

In normal operation, the signals arriving over the bus and the process interface are processed in accordance with the instructions contained in the structure list.

In line with these instructions, commands are output to the switchgear, and checkback signals indicating the process status are transmitted via the bus.

Modification of the parameter and limit value lists

The parameters and limit values can be changed from the PDDS (see ”Limit value list” and ”Parameter list”).

Modification of the structure and address lists

The structure and address lists can be transferred to the PDDS, modified there and transferred back to the module. To do so, the following procedure should be followed:

- The module should be in the EEPROM mode
- copy the complete user program from the EEPROM to the RAM, using the PDDS command ”KOP”
- transfer the list to be changed from the EEPROM (or RAM) to the PDDS, modify
- transfer the modified list to the module, which involves automatic storing in the RAM
- switch the module from EEPROM operation to RAM operation, using PDDS command ”UMS”, test new list
- to make new changes, switch again to EEPROM operation, repeat procedure.

Upon successful completion of the test, the complete user program can be transferred from the RAM to the non−volatile EEPROM, using either of the following commands:

- PDDS command ”Save” (SAV) or
- PDDS commands ”Copy from RAM to EEPROM” (KOP) and ”Switch over from RAM to EEPROM” (UMS)

”Save” effects copying of the lists and subsequent automatic switchover to EEPROM, without impairing processing on the module and command output.

Following a switchover operation with command UMS (from RAM to EEPROM and from EEPROM to RAM), the user lists in the RAM and EEPROM are compared. Should any deviation be detected, the controller and the binary group controls are switched to ”Manual”, the memories and timers are reset, and the commands present at the process interface are deactivated. For changed addresses of module inputs (EGn), the associated entries in the shared memory are set to zero until new data are received for the first time after switchover. If the lists are identical, processing will continue without any interruption.

Structure, address, parameter and limit value lists

For redundant operation, all of the lists contained in the module (structure, address, parameter and limit value lists) must be identical in the two redundant units. This can be ensured by the user with the aid of the PDDS.

Simulation

The PDDS permits constant values to be specified for up to 32 individual module signals. These simulation data are stored in the EEPROM in the EEPROM mode and in the RAM in the RAM mode.

The simulation data are also copied when the user lists are transferred from RAM to EEPROM and vice versa.

The simulation lists concerned are preserved in any changeover between RAM and EEPROM.

On cancellation of a simulation process via the PDDS, the simulation data are deleted and the module continues to operate with the data received over the bus or generated in the module.

When simulating redundant operation, the module signals simulated for the two redundant units must be indentical. This is ensured using the PDDS.

Checksum

A checksum for all active lists (structure, address, parameter, and limit value lists) in the EEPROM or RAM as well as the module firmware is formed in the module. This checksum can be used to verify that the contents of the lists in the on−line and the standby units are identical. The checksums can be displayed by the PDDS.

Command functions

Actuation from the control room

The module is controlled via the bus and does not have any hard−wired control room interfaces.

Actuation by a higher−level automatic system

A higher−level automatic system controls the module via the bus.

Release and protective commands

The logic combinations for release and protective commands are specified as required for the plant involved.

Command output

The commands for the drive control functions (binary control or step control) to which the process interfaces were assigned are output via relay outputs B11/B12 ... B41/B42. These actuate, in conjunction with the command outputs BV1 ... BV4 common to both command outputs, coupling relays on a two−channel basis.

The voltage for the command outputs B11/B12 ... B41/B42 is derived for each function unit from a separate, module−internal voltage.

The outputs are short−circuit−proof, protected against mutual interference, and provided with a protective circuit.

Checkback signals from the process

The drive−related checkback signals from the process, which are used by the drive control functions, can be connected via the module's hardware inputs (see Function diagram and Connection diagrams)

Operating modes

The module incorporates all function blocks required for the binary control, analog control and signal processing tasks on the drive, group and unit control levels. A set of function blocks is specified as "Operating mode" for a particular application. This is done by means of function block TXT1 which must appear at the top of the structure list, followed by text elements TXT for function designations.

Operating mode	Module cycle time	Input TXT1
Binary control (and analog basic functions)	variable up to max. 700 ms	STR
Analog control (and binary control)	fixed: 50, 100 150, 200 or 250 ms	REG, x x = 50 ms x = 100 ms x = 150 ms x = 200 ms x = 250 ms
Signal conditioning with disturbance bit output	fixed: 250 ms	MWV

The module cycle time is determined by the number and type of function blocks entered in the structure list. The cycle times indicated as "fixed" are minimum times. They apply whenever the time resulting from the structure list is shorter.
The actually required time is filed in register 205 and can be read out via the PDDS.

The following set of functions can be implemented for each module:

- 4 group control functions, e.g. GSA/GSV functions or
- 4 drive control functions, e.g. ASI/ASE/ASS/ASM functions or
- combinations of drive and group controls are permissible. The module cycle time should be considered.

In the analog control mode, the following combinations are possible, depending on the module cycle time chosen:

Operating mode **Analog control** (and binary control)	REG 50 ms	REG 100 ms		REG 150 ms			REG 200/ 250 ms			
ASI	1	1	2	1	2	3	1	2	3	4
ASE, ASM, ASS	–	≤ 3	–	≤ 3		–	≤ 3			–

The module cycle time should be considered.

The 4 process interfaces of the modules including command outputs are assigned to the drive control functions ASE/ASS/ASM/ASI whose inputs annunciations from the process, (PRO), are marked "VPn" in the address list. The following allocation applies:

n = 1 Process interface 1
n = 2 Process interface 2
n = 3 Process interface 3
n = 4 Process interface 4

The module is connected to the control room through the process operator station.

Function blocks

Synchronism

Function blocks with memory functions are synchronized by means of synchronizing telegrams transmitted by the on−line unit to the standby unit. The contents of the telegrams depends on the function block concerned. In the event mode, synchronizing telegrams are transmitted whenever a change occurs. All synchronizing telegrams are destination telegrams with data type 27. They do not have to be configured.

The synchronizing telegrams are also transmitted cyclically (in each remote bus cycle, all synchronizing telegrams of one station are transmitted) in the background for the purpose of monitoring the transmission path of the synchronizing function. If the monitor is activated, this is indicated by the annunciation "synchro−monitoring responded".

Synchronization after module restart following connection of supply voltage, insertion of the module, or reloading of user lists

After each restart, the on−line module is put in an operational state and immediately starts performing its processing functions and transmitting synchronizing telegrams to the standby unit.

When a standby unit is restarted, it is put in an operational state. The unit's disturbance lamp ST will light and the annunciation "synchro−monitoring responded" will be present in the diagnosis register until the unit has received the required synchronizing telegrams. When all synchronizing telegrams have been received, this means that the processing statusses of the on−line and standby units are identical.

Function blocks for the operating mode Binary control (STR)

This operating mode provides the function blocks for all binary control functions on the drive, group and unit control levels. Additional analog basic functions are available.

The module cycle time is variable, i.e. it is strictly determined by the function blocks used.

In this operating mode, no disturbance bits are transmitted for analog values, except at the output of the function block GRE.

Function blocks	**Abbrev.**
BINARY FUNCTIONS	
Switch−off delay element	ASV
2 of 3 selection, binary	B23
2 of 4 selection, binary	B24
M of N selection, binary	BMN
Extended bit marshalling	BRA1
Extended bit marshalling	BRA2
Dual−BCD converter	DBC1
Dual−Decimal converter	DDC
Dynamic OR gate	DOD
Switch−on delay element	ESV
Monostable flipflop ”Break”	MOA
Monostable flipflop ”Constant”	MOK
OR gate	ODR
RS flipflop	RSR
AND gate	UND
Counter	ZAE
GROUP CONTROL	
Group control function for sequential control	GSA2
Group control function for logic control	GSV
Criteria indication	KRA1
Criteria indication without watchdog	KRA3
Step function	SCH1
Preselect function, 2−fold	VW2
Preselect function, 3−fold	VW3
Preselect function, 4−fold	VW4
Select switch, 4−fold	WS4
Select switch, 4−fold	WS41
DRIVE CONTROL	
Drive control function Unidirectional drive	ASE1
Drive control function Solenoid valve	ASM1
Drive control function Actuator	ASS1

Function blocks	**Abbrev.**
LIMIT SIGNAL ELEMENTS	
Limit signal element for upper limit value	GOG
Limit signal element for lower limit value	GUG
Limit signal generation	GRE
ANALOG FUNCTIONS	
Absolute value generator	ABS
Limiter	BEG
Divider	DIV
Function generator	FKG
Factor variation	KVA
Maximum value selector	MAX
Minimum value selector	MIN
Multiplier	MUL
Monitoring and select function	MVN
Delay element	PT0
Delay element	PT1
Square root extractor	RAD
Summing multiplier	SMU
Fault flag suppression	SZU
Time variation	TVA
Change−over switch	UMS
PUSHBUTTON SELECTION FUNCTIONS	
Pushbutton selection	TAW
Pushbutton selection and target value presetting	TAZ
ORGANISATION FUNCTIONS	
Text element for designation and note	TXT
Text element for operating mode	TXT1
PROCESS INPUT/OUTPUT FUNCTIONS	

Note:

The process input/output function blocks are available from version P0003 on upwards.

Input of binary process signals	EP01
Output of binary process signals	AP01

The exact specification of the function blocks as well as the procedure for structuring are shown in the function block descriptions.

Function blocks for the operating mode Analog control (REG)

This operating mode provides the function blocks for all analog control functions for single variable and master control. In addition, the function blocks for drive and group control are available.

In this operating mode, no disturbance bits are transmitted for analog values, except at the output of the function block GRE.

The module cycle time can be preset in steps as fixed minimum time (see inputs in text element TXT1).
When implementing several control loops on one module, it should be noted that the cycle time of the module increases accordingly.

To ensure precise positioning in the case of single variable step controllers, the regulating time of the actuator (from 0 – 100 %) must correspond to 200 times the module cycle time, e.g.

Regulating time > 10 s for a cycle time of 50 ms

Function block	**Abbrev.**
BINARY FUNCTIONS	
Switch–off delay element	ASV
2 of 3 selection, binary	B23
2 of 4 selection, binary	B24
M of N selection, binary	BMN
Extended bit marshalling	BRA1
Extended bit marshalling	BRA2
Dual–BCD converter	DBC1
Dual–Decimal converter	DDC
Dynamic OR gate	DOD
Switch–on delay element	ESV
Monostable flipflop "Break"	MOA
Monostable flipflop "Constant"	MOK
OR gate	ODR
RS flipflop (with reset input dominant)	RSR
AND gate	UND
Counter	ZAE
DRIVE CONTROL	
Drive control function Unidirectional drive	ASE1
Drive control function Incremental output with expanded capabilities	ASI2
Drive control function Solenoid valve	ASM1
Drive control function Actuator	ASS1
LIMIT SIGNAL ELEMENTS	
Limit signal element for upper limit value	GOG
Limit signal generation	GRE
Limit signal element for lower limit value	GUG

Function block	**Abbrev.**
ANALOG FUNCTIONS	
Absolute value generator	ABS
Limiter	BEG
Divider	DIV
Function generator	FKG
Integrator	INT1
Factor variation	KVA
Maximal value selector	MAX
Minimal value selector	MIN
Multiplier	MUL
Monitoring and select function	MVN
Differentiator with P–DT1 action	PDT
Delay element	PT0
Delay element	PT1
Square root extractor	RAD
Summing multiplier	SMU
Time variation	TVA
Change–over switch	UMS
ANALOG CONTROL	
Manual station	HST1
PID Controller	PID3
PI Controller	PIR3
P Controller	PRE
Differentiator with derivative action	PTV
Setpoint integrator	SWI1
Setpoint adjuster	SWV1
Fault flag suppression	SZU
PUSHBUTTON SELECTION FUNCTIONS	
Pushbutton selection	TAW
Pushbutton selection and target value presetting	TAZ
ORGANISATION FUNCTIONS	
Text element	TXT
Text element for operating mode	TXT1
PROCESS INPUT/OUTPUT FUNCTIONS	
Note:	
The process input/output function blocks are available from version P0003 on upwards.	
Input of binary process signals	EP01
Output of binary process signals	AP01

The exact specification of the function blocks as well as the procedure for structuring are shown in the function block descriptions.

Function blocks for the operating mode Signal conditioning (MWV)

This operating mode provides analog computing functions and basic binary functions. A separate complete function block ”ENT” is available to calculate the enthalpy. In addition, binary and analog control functions are available.

In this operating mode, any disturbance bits set to ”1” in incoming telegrams are taken over into data telegrams which are calculated from them and subsequently transmitted.

The minimum module cycle time is permanently set to 250 ms.

Function module	**Abbrev.**
BINARY FUNCTIONS	
Switch−off delay element	ASV
2 of 3 selection, binary	B23
2 of 4 selection, binary	B24
M of N selection, binary	BMN
Extended bit marshalling	BRA1
Extended bit marshalling	BRA2
Dual−BCD converter	DBC1
Dual−Decimal converter	DDC
Dynamic OR gate	DOD
Switch−on delay element	ESV
Monostable flipflop (Break)	MOA
Monostable flipflop (Constant)	MOK
OR gate	ODR
RS flipflop (with reset input dominant)	RSR
AND gate	UND
Counter	ZAE
LIMIT SIGNAL ELEMENTS	
Limit signal element for upper limit value	GOG
Limit signal generation	GRE
Limit signal element for lower limit value	GUG

Function block	**Abbrev.**
ANALOG FUNCTIONS	
Absolute value generator	ABS
Limiter	BEG
Divider	DIV
Enthalpy function	ENT
Function generator	FKG
Integrator	INT1
Factor variation	KVA
Maximal value selector	MAX
Minimal value selector	MIN
Multiplier	MUL
Monitoring and select function	MVN
Differentiator with P−DT1 action	PDT
Delay element	PT0
Delay element	PT1
Differentiator with derivative time	PTV
Square root extractor	RAD
Summing multiplier	SMU
Time variation	TVA
Change−over switch	UMS
ORGANISATION FUNCTIONS	
Text element	TXT
Text element for operating mode	TXT1
PROCESS INPUT/OUTPUT FUNCTIONS	

Note:

The process input/output function blocks are available from version P0003 on upwards.

Input of binary process signals	EP01
Output of binary process signals	AP01

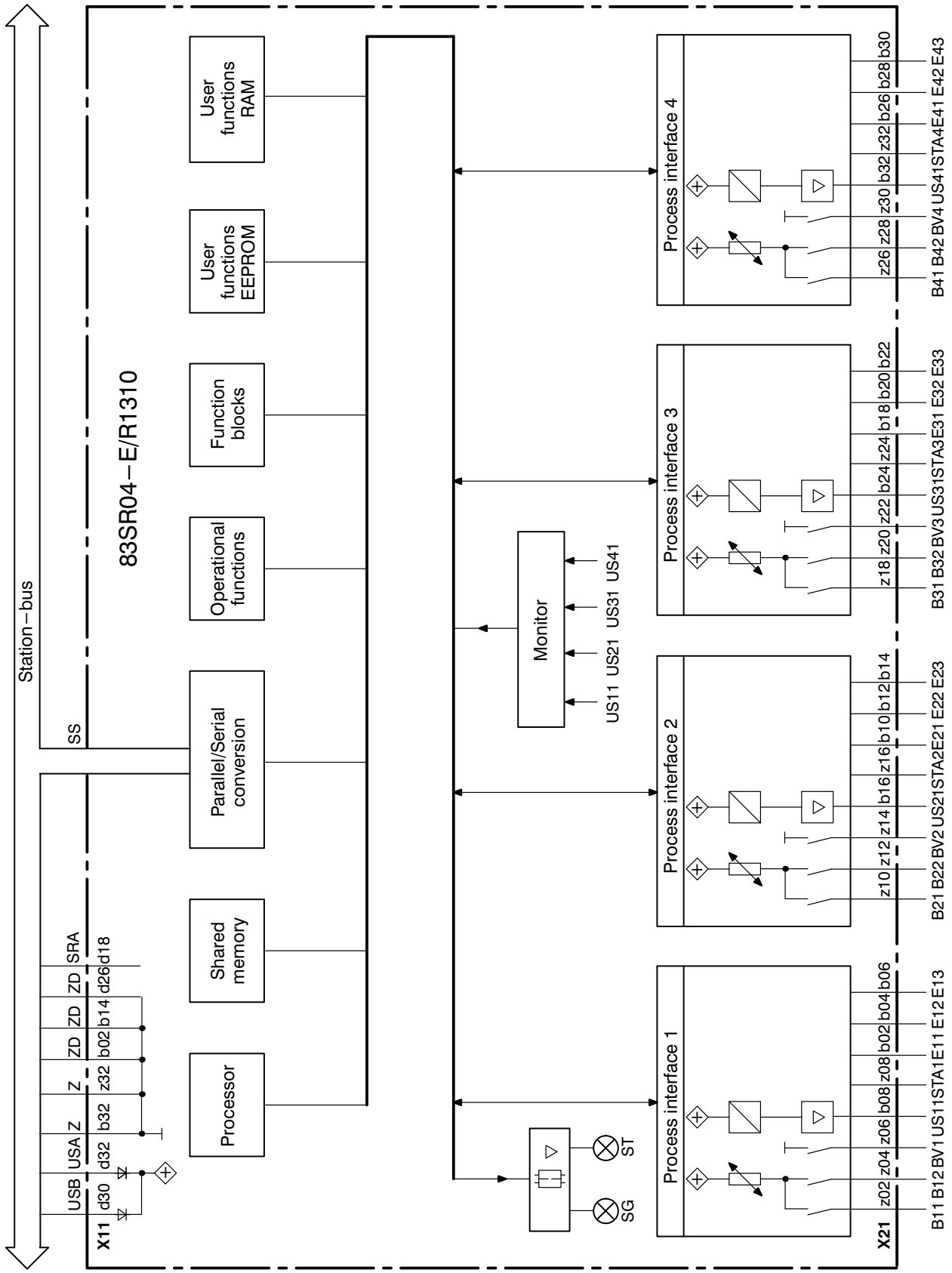
The exact specification of the function blocks as well as the procedure for structuring are shown in the function block descriptions.

Functional diagram

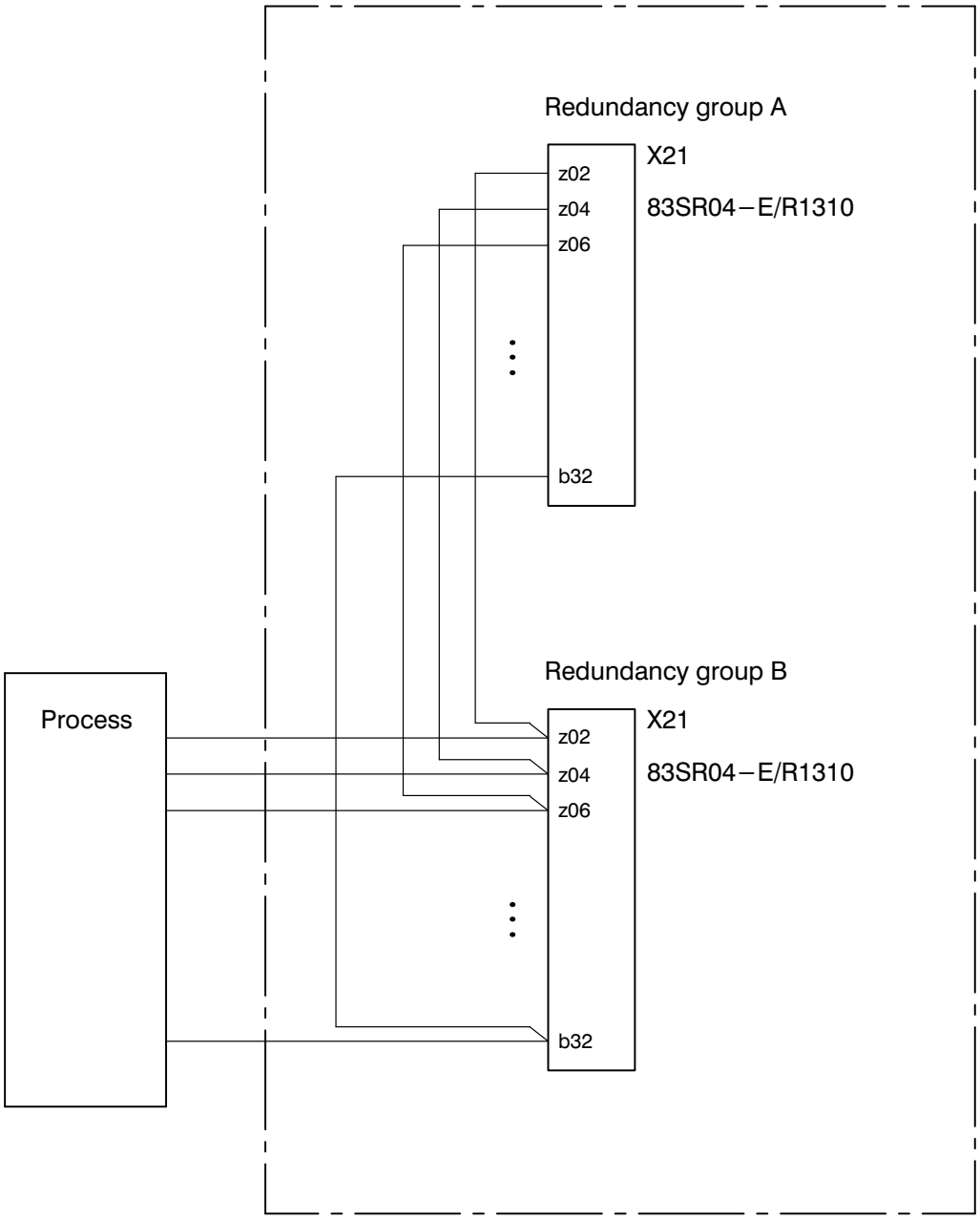
Terminal designations

The printed circuit board is equipped with connectors X11 and X21.

Connector X21 incorporates all process inputs and outputs. Connector X11 contains the station−bus interface and the operating voltages USA and USB.

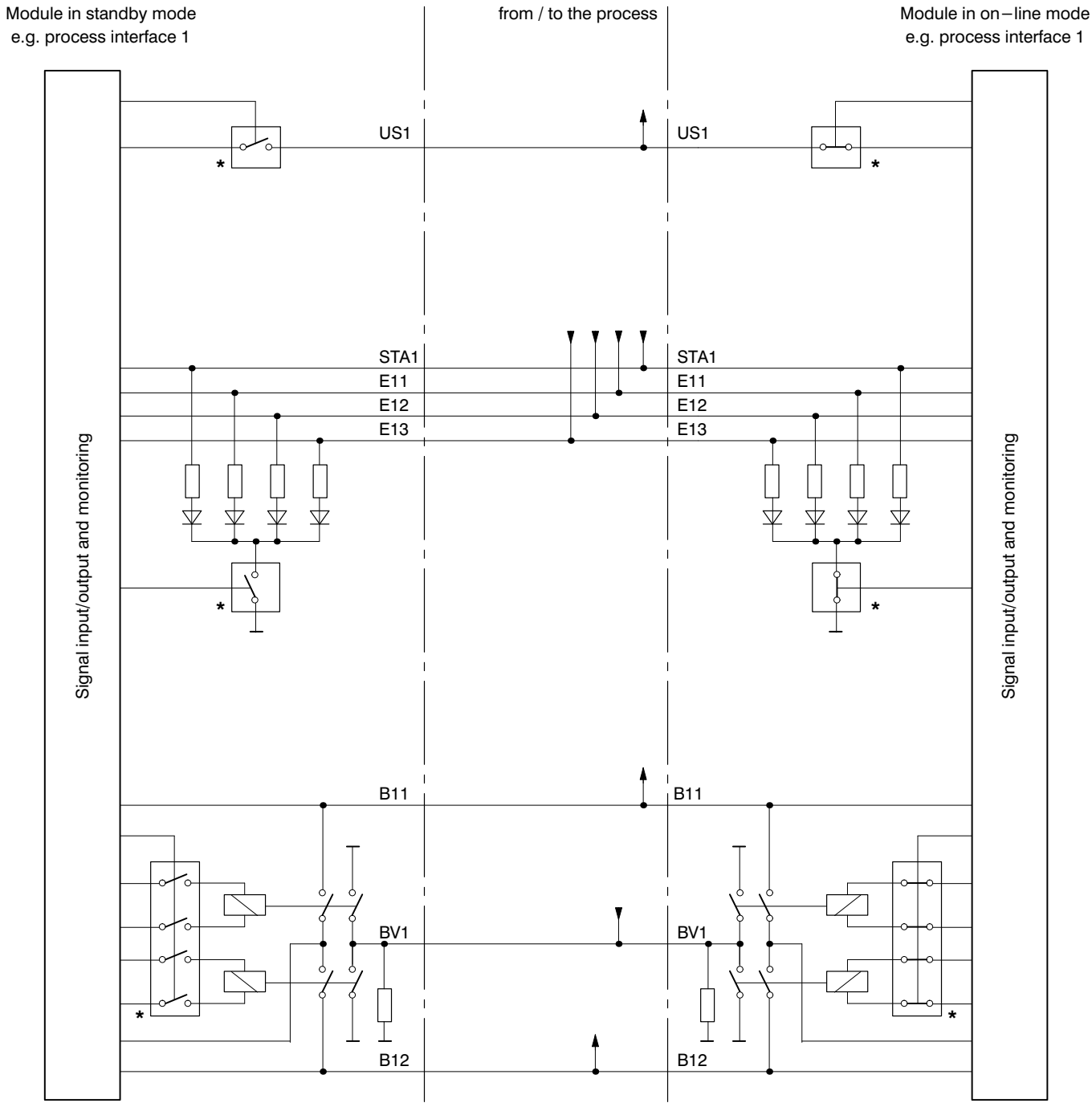


Basic connection diagram, redundancy wiring



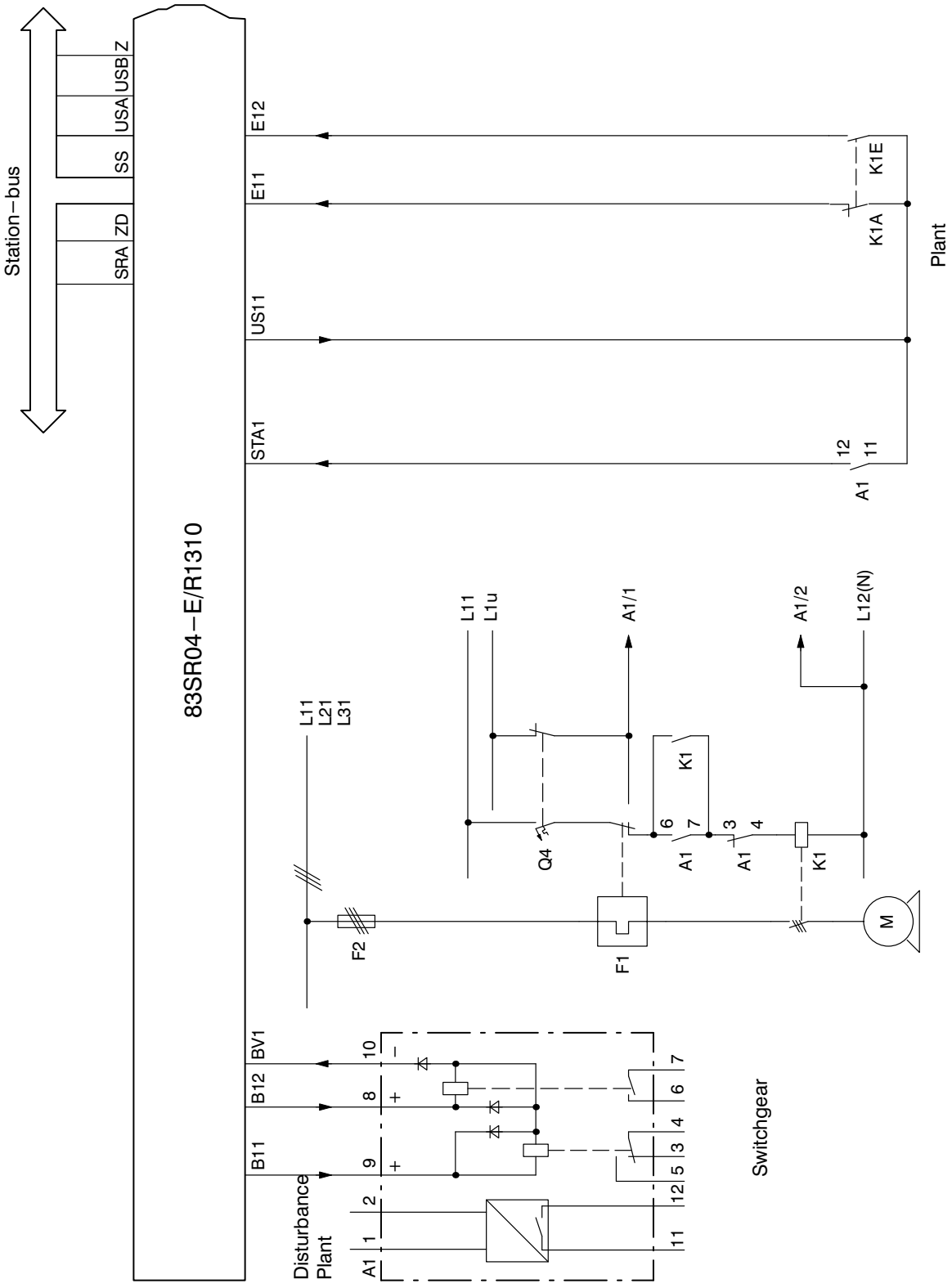
Basic connection diagram, inputs and outputs in a redundant disign

83SR04−E/R1310

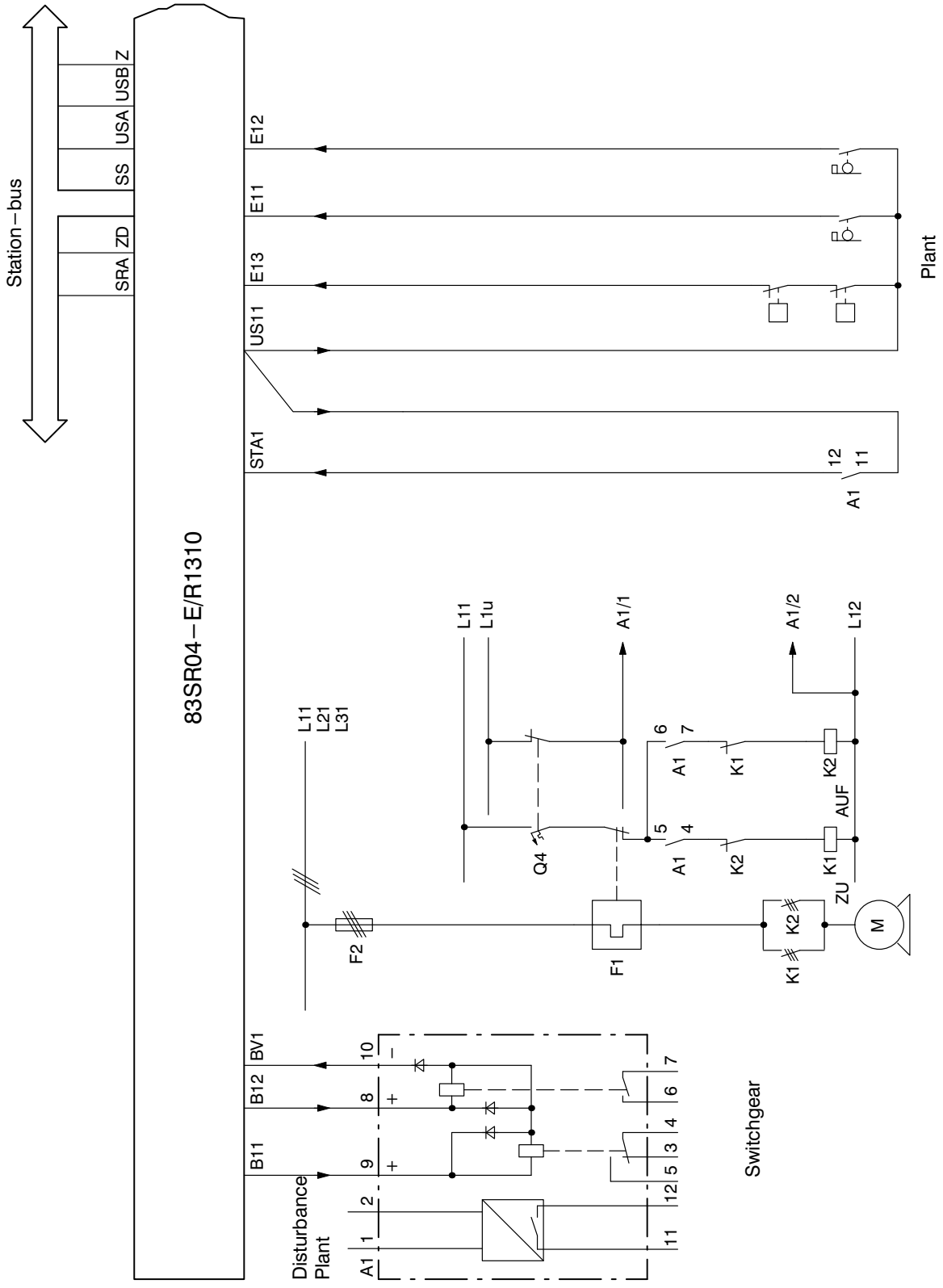


* electronic switch

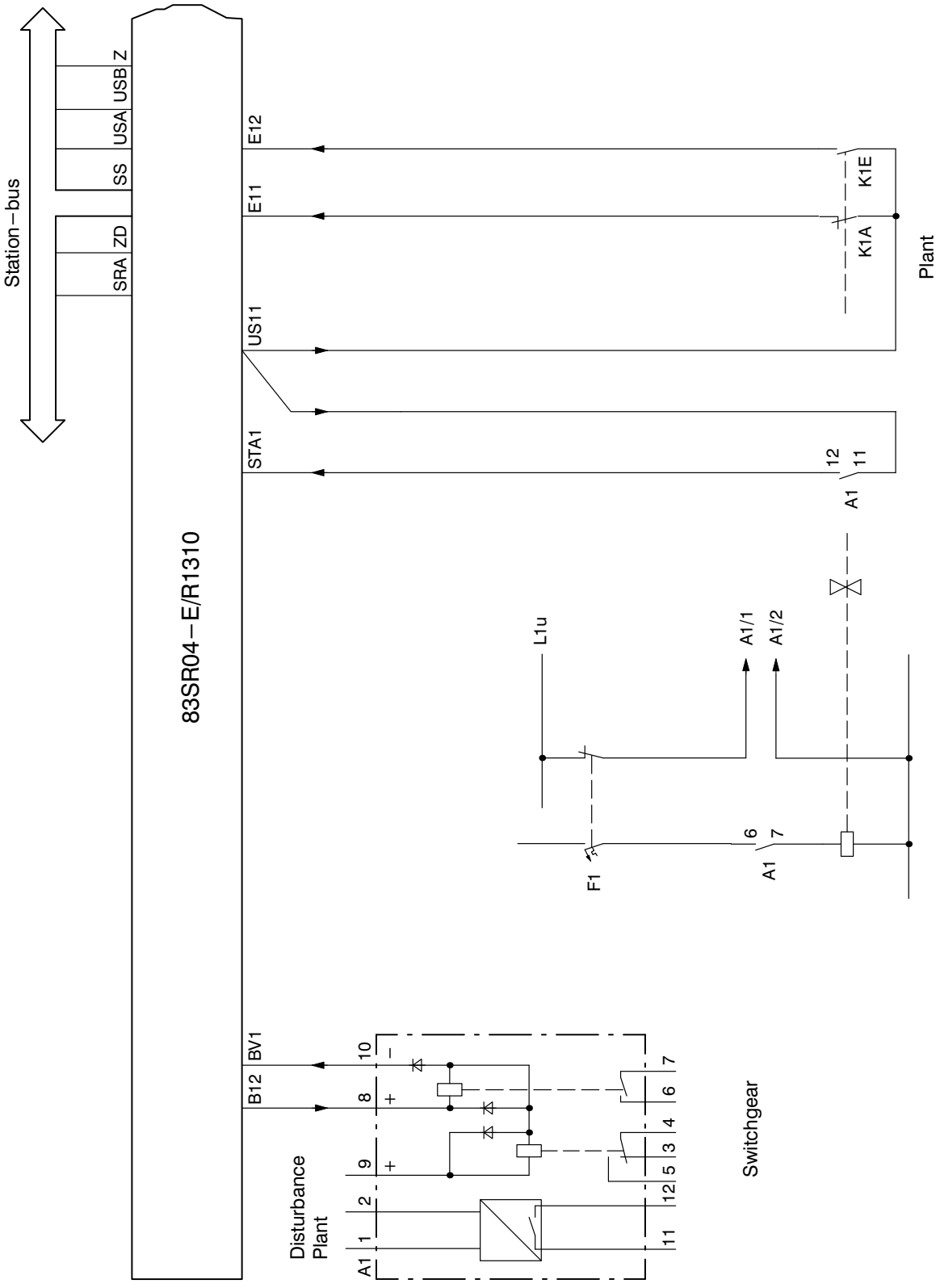
Connection diagram Unidirectional drive (function unit 1)



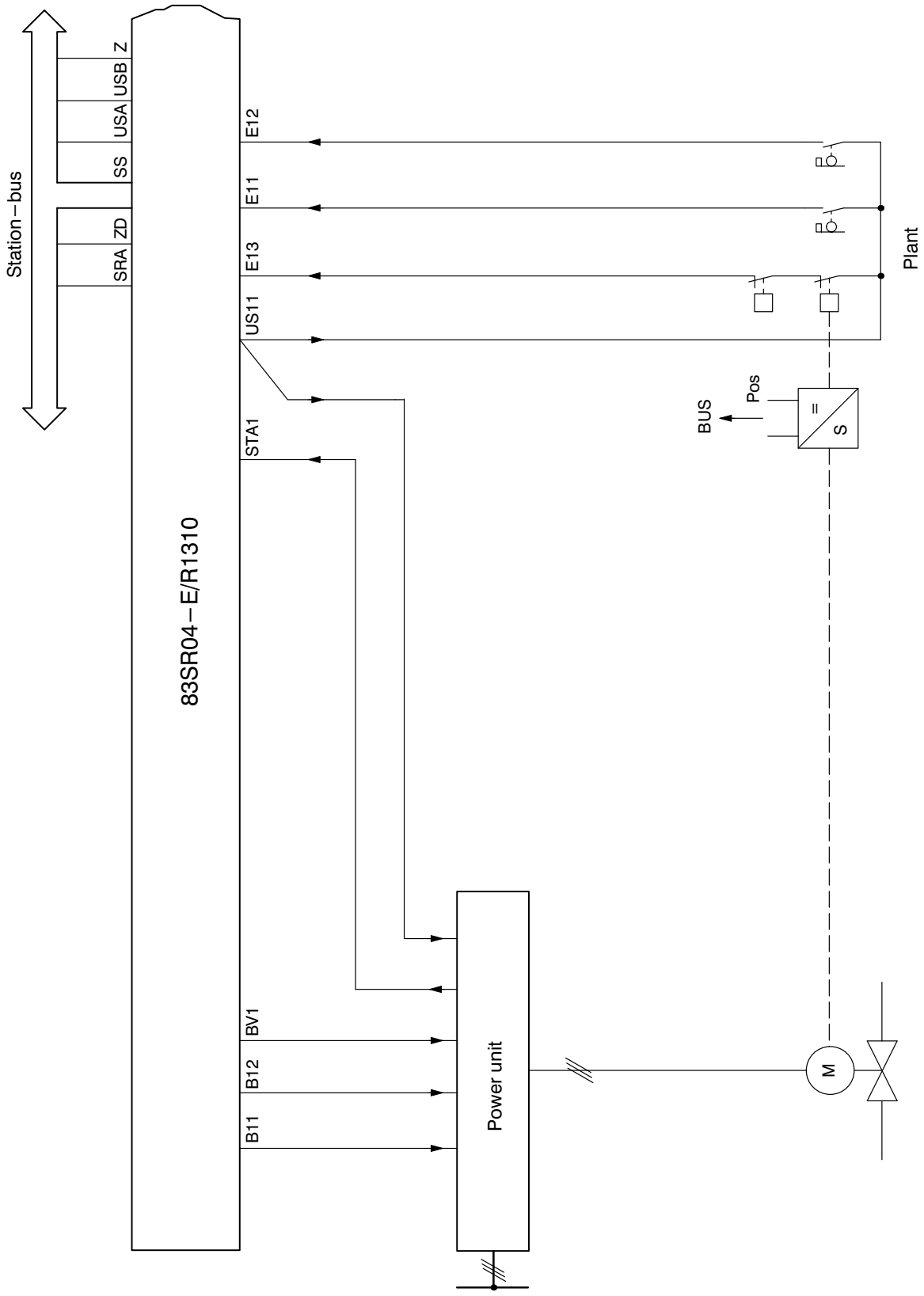
Connection diagram Actuator (function unit 1)



Connection diagram Solenoid valve (function unit 1)



Connection diagram 3−step controller (function unit 1)



Mechanical design

Board size: 6 units, 1 division, 160 mm deep

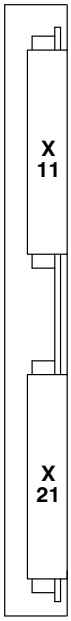
Connector: to DIN 41 612

1 x for station−bus connection,
48−pole edge−connector type F
(connector X11)

1 x for process connection,
32−pole edge−connector type F
(connector X21)

Weight: approx. 0.55 kg

View of the connector side:

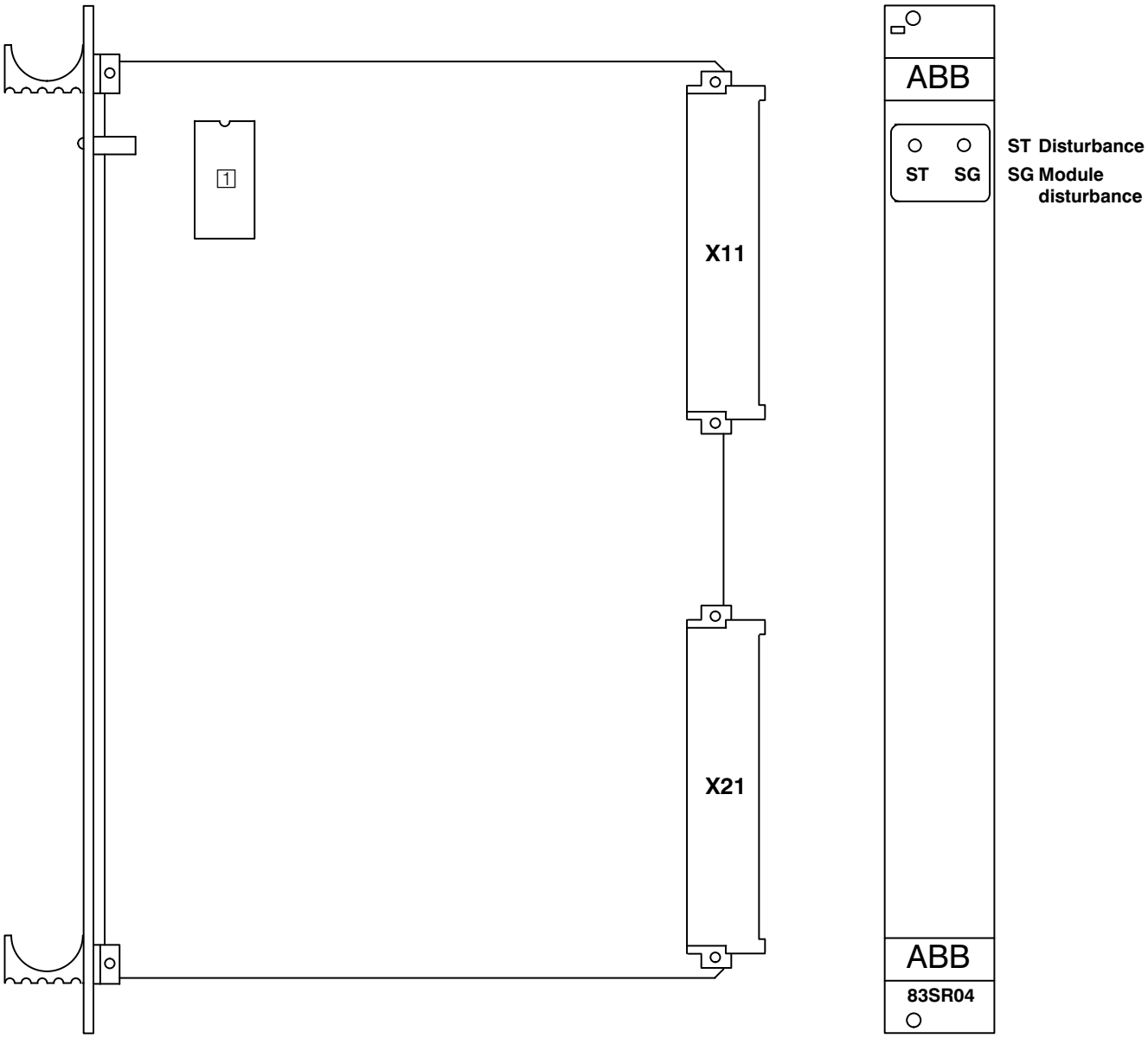


Contact allocation of process connector X21

View of the contact side:

	b	*z*
02	E11	B11
04	E12	B12
06	E13	BV1
08	US11	STA1
10	E21	B21
12	E22	B22
14	E23	BV2
16	US21	STA2
18	E31	B31
20	E32	B32
22	E33	BV3
24	US31	STA3
26	E41	B41
28	E42	B42
30	E43	BV4
32	US41	STA4

Side view and view of module front



1 EPROM programmed, order number: GJR2390243Pxxxx
xxxx = Position number indicating the applicable program version

Technical data

In addition to the system data, the following values apply:

Power supply

Operating voltage Module		USA/USB = 24 V
Current consumption		IS = 145 mA + output currents
Power dissipation,	on−line status	PV = 3.5 ... 7.0 W
	standby status	PV = 3.2 ... 3.5 W depending on operation voltage and configuration
Reference potential Process section		Z = 0 V
Reference potential Bus section		ZD = 0 V

Input values

Direct connections for 4 function units (FU)

Ex1	– Process checkback signal (EA/EZ)	OFF/CLOSED	5 mA at 48 V
Ex2	– Process checkback signal (EE/EO)	ON/OPEN	5 mA at 48 V
Ex3	– Torque monitor	CLOSED/OPEN	5 mA at 48 V
STAx	– Disturbance in switchgear		5 mA at 48 V

x from 1 to 4

Output values

CONTACT VOLTAGES

Contact voltages Process section for the inputs Ex1, Ex2, Ex3 and STAx	US11 = 48 V / ≤ 30 mA US21 = 48 V / ≤ 30 mA US31 = 48 V / ≤ 30 mA US41 = 48 V / ≤ 30 mA

x from 1 to 4

The outputs are short−circuit−proof and non−interacting.

PROCESS INTERFACE

Voltage supply of the 4 function units for the command outputs Bx1 and Bx2	24 V
The outputs are short−circuit−proof and non−interacting and are provided with a protective network	
	Loading capacity
Bx1 – Command output for OFF/CLOSE	IS ≤ 80 mA
Bx2 – Command output for ON/OPEN	IS ≤ 80 mA
BVx – Common command output for Bx1/Bx2 (wired return line)	IS ≤ 80 mA
For the connected load resistor the following limits apply	360 Ω ≤ R_{load} ≤ 15 kΩ
Service life of the relay output stages	≥ 20 million switching cycles

Output values

COUPLING RELAY AND POWER DRIVERS
IN THE SWITCHGEAR

Wiring:

The wiring from the 83SR04 to the switchgear is laid down in a cable specification to suit the plant.
The max. length of the line (outgoing and return lines) is 600 m for a cross−section of 0.5 mm^2.

The following coupling relays and power drivers can be used:

Coupling relay R513
Power driver with semiconductor LU370
or coupling relays and power drivers
with the same technical data.

Noise immunity

ESD acc. to IEC 801/2	8 kV to front panel
EMC acc. to IEC 801/4	1 kV burst
Destruction acc. to IEC 801/5, draft doc.: IEC TC65(Sec)137	1 kV to reference potential

ORDERING DATA

Order no. for complete module:

Type designation: 83SR04−E/R1310 Order number: GJR2390200R1310

Technical data are subject to change without notice!

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Printed in Germany (DEPPC/R21 0796 0,3 BID)